HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Docket No.: 200208727-1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Christopher A. Poirier et al.

Application No.: 10/644,625 | Confirmation No.: 7519

Filed: August 20, 2003 | Art Unit: 2825

For: A SYSTEM FOR AND METHOD OF CONTROLLING A VLSI ENVIRONMENT | Examiner: S. Whitmore

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under 37 C.F.R. § 41.37(a), this brief is filed not more than two months after the Notice of Appeal filed in this case on December 22, 2006, and is in furtherance of said Notice of Appeal.

The fees required under 37 C.F.R. § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Limited Partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 32 claims pending in application.

B. Current Status of Claims

1. Claims canceled: None

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-32

4. Claims allowed: None

5. Claims rejected: 1-32

C. Claims On Appeal

The claims on appeal are claims 1-32.

IV. STATUS OF AMENDMENTS

Appellant did not file a Response after the Office Action mailed on October 17, 2006 (hereinafter the "Final Action"). As such, the claims on Appeal are as they were in the response filed on July 27, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the separately argued claims involved in the Appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. It should be noted that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element.

Embodiments of the invention according to claim 1 provides a system (Figure 1, element 100, paragraph 18) comprising: an integrated circuit (paragraphs 2, 6, and 13) on a VLSI die (paragraphs 13-14); and an embedded micro-controller (Figure 1; element 103; paragraphs 6, 13, 18, and 28) constructed on the VLSI die, the micro-controller adapted to monitor (e.g., via elements 106-107, 109, 111-113, 115-116, and 116a-c of Figure 1; see paragraphs 18-21 and 23-25) and control (paragraphs 14-17) the VLSI environment (paragraph 13) to optimize the integrated circuit operation (paragraphs 22-23 and 27); wherein said embedded micro-controller monitors temperatures at a plurality of locations (e.g., at elements 106-107, 109, and 111 of Figure 1; see paragraphs 18-21) on the integrated circuit.

Embodiments of the invention according to claim 8 provide a method (Figure 3; paragraph 35) for monitoring (e.g., via elements 106-107, 109, 111-113, 115-116, and 116a-c of Figure 1; see paragraphs 18-21 and 23-25) and controlling (paragraphs 14-17) an integrated circuit (paragraphs 2, 6, and 13) comprising: providing (Figure 3, element 301; paragraph 35) an embedded micro-controller (Figure 1; element 103; and paragraphs 6, 13, 18, and 28) on a same VLSI die (paragraphs 13-14, and 18) as the integrated circuit; and monitoring (e.g., via elements 106-107, 109, 111-113, 115-116, and 116a-c of Figure 1; see paragraphs 18-21 and 23-25) and controlling (Figure 3; element 302; paragraphs 35; see also paragraphs 14-17) a VLSI environment (paragraph 13) of the integrated circuit with the embedded micro-controller; wherein said embedded micro-controller monitors temperatures at a plurality of locations (e.g., at elements 106-107, 109, and 111 of Figure 1; see paragraphs 18-21) on the integrated circuit.

Embodiments of the invention according to claim 16 provide a computer program product comprising a computer usable medium having computer readable program code embedded therein, the computer readable program code comprising: code (firmware 115, Figure 1, paragraph 23) for controlling an embedded micro-controller (element 103, Figure 1, paragraphs 6, 13, 18, and 28) constructed on a VLSI integrated circuit die (paragraphs 13-14, and 18) with a processor (e.g., cores 101 and 102, paragraphs 2, 6, and 13), wherein the micro-controller monitors and controls a VLSI environment (paragraph 13) of the processor; where said embedded micro-controller monitors temperatures at a plurality of locations (Figure 1; elements 106-107, 109, and 111; and paragraphs 18-21) on the integrated circuit.

Embodiments of the invention according to claim 24 provide a system (Figure 1, element 100, paragraph 18) for monitoring (e.g., via elements 106-107, 109, 111-113, 115-116, and 116a-c of Figure 1; see paragraphs 18-21 and 23-25) and controlling (paragraphs 14-17) an integrated circuit (paragraphs 2, 6, and 13) comprising: means for providing (Figure 3; element 301; paragraph 35) an embedded micro-controller (Figure 1; element 103; paragraphs 6, 13, 18, and 28) on a same VLSI die (paragraphs 13-14, and 18) as the integrated circuit; and means for monitoring and controlling a VLSI environment (paragraph 13) of the integrated circuit with the embedded micro-controller; wherein said embedded micro-controller monitors temperatures at a

plurality of locations (e.g., at elements 106-107, 109, and 111 of Figure 1; see paragraphs 18-21) on the integrated circuit.

Embodiments of the invention according to claim 4 provide a system of claim 1 wherein the integrated circuit comprises two or more processor cores (core 0 and core 1, elements 101 and 102, Figure 1, paragraph 18), each core having a integer unit (elements 104 and 108, Figure 1, paragraph 18) and a floating point unit (elements 105 and 110, Figure 1, paragraph 18), the micro-controller further comprising: temperature sensors (elements 106-107, 109, and 111, Figure 1, paragraphs 18-21) at each of the integer units and floating point units on each of the cores.

Embodiments of the invention according to claim 14 provide the method of claim 8 wherein the integrated circuit is a processor (Figure 1, element 100, paragraph 18), the method further comprising monitoring, using the embedded micro-controller, a temperature in a first core (Figure 1 core 0, element 101, paragraph 18) of the processor; and transferring, using the embedded micro-controller, a processing workload (paragraph 21) from the first core to a second core (Figure 1 core 1, element 102, paragraph 18) of the processor in response (paragraph 21) to the temperature of said first core.

Embodiments of the invention according to claim 22 provide the computer program product of claim 16 further comprising: code for monitoring a temperature in a first core (Figure 1 core 0, element 101, paragraph 18) of the processor; and code for transferring a processing workload (paragraph 21) from the first core to a second core (Figure 1 core 1, element 102, paragraph 18) of the processor in response (paragraph 21) to the temperature of said first core.

Embodiments of the invention according to claim 28 provide the system of claim 24 wherein the integrated circuit is a processor (Figure 1, element 100, paragraph 18), the method further comprising: means for monitoring, using the embedded micro-controller, a temperature in a first core (Figure 1 core 0, element 101, paragraph 18) of the processor; and means for transferring, using the embedded micro-controller, a processing workload (paragraph 21) from

the first core to a second core (Figure 1 core 1, element 102, paragraph 18) of the processor in response (paragraph 21) to the temperature of said first core.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-3, 8-13, 16-21, 24-27, and 29-32 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,694,492 to Shakkarwar (hereinafter "Shakkarwar").

B. Claims 4, 14, 22, and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shakkarwar in view of U.S. Patent Application Publication No. 2003/0225999 to Rogenmoser et al. (hereinafter "Rogenmoser").

C. Claims 5, 15, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shakkarwar in view Korean Patent Publication 9405466 B1 to Kim (hereinafter "Kim").

VII. ARGUMENT

Appellant respectfully traverses the outstanding rejections of the pending claims, and requests that the Board reverse the outstanding rejections in light of the remarks contained herein. The claims do not stand or fall together. Instead, Appellant presents separate arguments for various independent and dependent claims. Each of these arguments are presented with separate headings and sub-headings as required by 37 C.F.R. § 41.37(c)(1)(vii).

A. Claims 1-3, 8-13, 16-21, 24-27, and 29-32 are rejected under 35 U.S.C. § 102(e) as being anticipated by Shakkarwar.

To anticipate a claim under 35 U.S.C. § 102, a single reference must teach each and every element of the claim. *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). As discussed below, Shakkarwar fails to teach each and every claim limitation. Therefore Appellant respectfully requests that the Board reverse these rejections.

1. Independent claims 1, 8, 16, and 24

Claims 1, 8, 16, and 24 recite "said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit." In the Final Action, the Examiner points to Shakkarwar, particularly at col. 4 lines 4-54 and col. 6 lines 39-62, as satisfying this limitation. In doing so, the Examiner opines "Shakkarwar discloses in lines 4-19 [of col. 4] that multiple areas under varying conditions (temperature variation and thermal management) of the integrated circuit are monitored and controlled by element 130." *See* Final Action, pg. 6. As an initial matter, Appellant points out that Shakkarwar does not disclose monitoring "multiple areas," as the Examiner suggests. Rather, Shakkarwar merely discloses applying test vectors to monitor the function of sub-components and applying multiple tests to determine IC characteristics under different conditions. *See* Shakkarwar col. 4, lines 16-19. Appellant acknowledges that Shakkarwar discloses a single thermal sensor 107, where a signal 124 is received at test controller 110 from sensor 107 and may be used to "assess thermal characteristics of central processing unit 102." *See* Shakkarwar, col. 6 lines 21-24. Also, as seen in Figure 1, thermal sensor 107 provides a single output to each of the power controller 108, internal controller 130, and test controller 110. Appellant points out that Shakkarwar's disclosure of a *single* sensor (thermal sensor 107) having a *single* output signal sent to a number of controllers (signal 117, 124, 138) does not teach monitoring temperatures at a plurality of locations. Also, Shakkarwar discloses that its thermal sensor can monitor thermal parameters of the IC; however, there is no indication that these thermal parameters are measured at more than one location. *See* Shakkarwar, col. 4 lines 21-29. As such, Shakkarwar fails to teach monitoring temperatures at a plurality of locations on the integrated circuit as set forth in the claims. Therefore, Appellant respectfully requests reversal of the rejection of record.

2. Dependent Claims 2-3, 9-13, 17-21, 25-27, and 29-32

Claims 2-3 and 29 depend from claim 1, claims 9-13 and 30 depend from claim 8, claims 17-21 and 31 depend from claim 16, and claims 25-27 and 32 depend from claim 24. Each of the dependent claims inherit every limitation of the claims from which they depend. As such, claims 2-3, 9-13, 17-21, 25-27, and 29-32 set forth limitations not taught by Shakkarwar, and are

allowable at least for the reasons set forth above with respect to claims 1, 8, 16, and 24. Further, these claims set forth limitations making them patentable in their own right. Therefore Appellant respectfully requests that the Board reverse these rejections.

a. *Dependent claim 6*

For example, claim 6 recites "fuses that provide hardware selection of VLSI integrated circuit environment parameters that are monitored by the embedded micro-controller." As an initial matter, Appellant notes that there is no rejection of record with respect to claim 6. Nevertheless, Appellant endeavors to point out that Shakkarwar does not teach or suggest this limitation. For instance, Shakkarwar merely discloses that its fuses may be used to implement a clock register or voltage register, which are programmed at the time the CPU die is tested. As such, Shakkarwar's fuses do not provide hardware selection of VLSI integrated circuit environment parameters that are monitored by the embedded micro-controller, as set forth in claim 6. Moreover, Rogenmoser and Kim do not appear to teach or suggest this limitation. Therefore, Appellant respectfully requests that the Board indicate the allowability of this claim.

b. *Dependent claim 7*

Claim 7 recites updateable or replaceable firmware, said firmware comprising algorithms for determining how to respond to temperature, power, voltage, or clock parameters. As an initial matter, Appellant notes that there is no rejection of record with respect to claim 7. Nevertheless, Appellant endeavors to point out that Shakkarwar does not teach or suggest this limitation. For instance, Shakkarwar merely discloses "a diagnostics program to verify responses from a CPU." *See* Shakkarwar at col. 6, lines 48-49. However, this diagnostics program is not a firmware, and even if it could be construed as such, the program is neither updateable nor replaceable. Further, Shakkarwar is wholly silent as to firmware comprising algorithms for determining how to respond to temperature, power, voltage, or clock parameters. Moreover, neither of Rogenmoser or Kim appear to teach or suggest this limitation. As such, Shakkarwar does not teach every limitation of Appellant's claimed invention. Therefore, Appellant respectfully requests that the Board indicate the allowability of this claim.

c. *Dependent claims 20 & 21*

Claims 20 and 21 recite "code for monitoring a temperature in a core of the processor." As best Appellant understands, the Examiner does not point out specifically where, in Shakkarwar, every limitation of claim 20 is satisfied. Instead, the Examiner merely states that Shakkarwar discloses the elements of the instant application. *See* Final Action, pgs. 5-6. Nevertheless, Appellant notes that Shakkarwar merely discloses that "a core of the processor" is CPU core 106. However, Shakkarwar shows thermal sensor 107 located outside of CPU core 106, such that the temperature monitored is outside of CPU core 106. *See* Shakkarwar at Fig. 1. As such, Shakkarwar, at best, teaches monitoring a temperature outside a core of the processor, yet does not teach monitoring a temperature in a core of the processor. Therefore, Appellant respectfully requests the Board reverse the 35 U.S.C. § 102(e) rejection of record.

d. *Dependent claims 29-32*

Claims 29-32 recite "said embedded micro-controller is further adapted to detect a difference in temperatures between said plurality of locations on the integrated circuit and redistribute workload in response to said temperature difference." Appellant points out that Shakkarwar does not teach or suggest this limitation. That is, Shakkarwar discloses a single thermal sensor 107, where a signal 124 received at test controller 110 from sensor 107 may be used to "assess thermal characteristics of central processing unit 102." *See* Shakkarwar, col. 6 lines 21-24. Appellant points out that Shakkarwar's disclosure of a *single* sensor (thermal sensor 107) having a *single* output signal sent to a number of controllers (signals 117, 124, 138) does not teach detecting a difference in temperatures between a plurality of locations. Also, Shakkarwar discloses that its thermal sensor can monitor thermal parameters of the IC; however, there is no indication that these thermal parameters are measured at more than one location. *See* Shakkarwar, col. 4 lines 21-29. Even if Shakkarwar could be construed to disclose detecting a difference in temperature at locations on the integrated circuit (which Appellant does not concede as accurate), there is no mention of redistributing workload in response to a temperature difference. At best, Shakkarwar changes operating voltage or frequency for an integrated circuit. However, Shakkarwar does not teach that its operating voltage or frequency is changed in

response to temperature differences. Moreover, Shakkarwar's changes apply to the entire IC; as such, there is no "redistribution" as set forth in the claims. Therefore, Appellant respectfully requests that the Board reverse the 35 U.S.C. § 102(e) rejection of record.

B. Claims 4, 14, 22, and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shakkarwar in view of Rogenmoser.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. Without conceding that the first or second criteria is satisfied, the Appellant respectfully asserts that the Examiner's rejection fails to satisfy the third criteria.

Failure to Teach or Suggest Every Claim Limitation

Claim 4 depends from claim 1, claim 14 depends from claim 8, claim 22 depends from claim 16, and claim 28 depends from claim 24. Each of claims 4, 14, 22, and 28 inherit every limitation of the claims from which they depend. As shown above, Shakkarwar fails to teach or suggest "said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit." Moreover, Rogenmoser is not relied upon to teach or suggest this missing limitation, nor does it do so. As such, claims 4, 14, 22, and 28 set forth limitations not taught or suggested by the Examiner's proposed combination, and are allowable at least for the reasons set forth above with respect to claims 1, 8, 16, and 24. Further, these claims set forth additional limitations making them patentable in their own right. Therefore, Appellant respectfully requests that the Board indicate the allowability of these claims.

1. Dependent Claim 4

Claim 4 recites "temperature sensors at each of the integer units and floating point units on each of the cores." The Examiner acknowledges that "Shakkarwar does not specifically

disclose the IC having two or more processor cores each with integer and floating point unit[s] and temperature sensors at each of the units." *See* Final Action, pg. 4. Instead, the Examiner relies upon Rogenmoser as teaching these limitations. Appellant respectfully points out that Shakkarwar teaches a processor 102 containing a single thermal sensor 107 located outside of CPU core 106, *see* Shakkarwar Figure 1 and col. 4 ll. 20-29, and that Rogenmoser teaches a processor 10 containing two integer units (22A-22B) and two floating point units (24A-24B). *See* Rogenmoser Figure 4. As such, the combination of Shakkarwar and Rogenmoser would, at best, provide Shakkarwar's single thermal sensor and Rogenmoser's two integer units and two floating point units, whereas the claim recites temperature sensors at each of the integer units and floating point units. Thus, Shakkarwar in view of Rogenmoser does not teach or suggest all limitations of claim 4. Accordingly, Appellant respectfully asserts that the rejection is improper and requests that it be reversed.

2. Dependent Claim 14 & 28

Claims 14 and 28 recite "the integrated circuit is a processor" and "a first core ... [and] a second core of the processor." In the Final Action, the Examiner acknowledges that "Shakkarwar does not specifically disclose the IC having two or more processor cores each with integer and floating point unit[s] and temperature sensors at each of the units." *See* Final Action, pg. 4. However, Rogenmoser does not satisfy this limitation either. That is, Rogenmoser, at Figure 4, merely depicts a block diagram of a processor (Rogenmoser's element 10, paragraph 14). Also, at Figures 2-3 Rogenmoser depicts block diagrams of integrated circuits having two or four processors 10 (Rogenmoser at paragraphs 2-3). As such, Rogenmoser teaches an integrated circuit having multiple processors, but Rogenmoser does not teach a processor having a first core and a second core. Thus, Shakkarwar in view of Rogenmoser does not teach or suggest all limitations of claims 14 and 28. Therefore, Appellant asserts that the rejection of claims 14 and 28 under 35 U.S.C. § 103(e) is improper and requests that the rejection be reversed.

Claims 14 and 28 also recite "monitoring ... a temperature in a first core of the processor." According to Shakkarwar, "a first core of the processor" is CPU core 106.

Moreover, Shakkarwar's Figure 1 shows thermal sensor 107 located outside of CPU core 106, such that the temperature monitored is outside of CPU core 106. As such, the combination of Shakkarwar and Rogenmoser would, at best, teach monitoring a temperature outside a core of the processor, yet does not teach monitoring a temperature in a first core of the processor. Thus, Shakkarwar in view of Rogenmoser does not teach or suggest all limitations of claims 14 and 28. Accordingly, Appellant respectfully asserts that the rejection is improper and requests that it be reversed.

3. Dependent Claim 22

Claim 22 recites "a first core ... [and] a second core of the processor." In the Final Action, the Examiner acknowledges that "Shakkarwar does not specifically disclose the IC having two or more processor cores each with integer and floating point unit[s] and temperature sensors at each of the units." *See* Final Action section 4, page 4. Instead, the Examiner relies upon Rogenmoser as teaching these limitations. However, Appellant respectfully points out that Rogenmoser's Figure 4 is a block diagram of a processor (i.e., Rogenmoser's element 10, paragraph 14). Further, Figures 2-3 are merely block diagrams of integrated circuits having two or four processors 10 respectively (Rogenmoser paragraphs 2-3). As such, Rogenmoser teaches an integrated circuit having multiple processors, but Rogenmoser does not teach that the processor has a first core and a second core. Thus, Shakkarwar in view of Rogenmoser does not teach or suggest all limitations of claim 22. Therefore, Appellant asserts that the rejection of claim 22 under 35 U.S.C. § 103 is improper and requests that the rejection be reversed.

Further, claim 22 recites "monitoring a temperature in a core of the processor." In reviewing Shakkarwar and Rogenmoser, Appellant asserts that the element, if any, that comes closest to meeting "a first core of the processor" is Shakkarwar's CPU core 106. Shakkarwar Figure 1 shows thermal sensor 107 located outside of CPU core 106, such that the temperature monitored is outside of CPU core 106. As such, the combination of Shakkarwar and Rogenmoser would teach monitoring a temperature outside a core of the processor, yet does not teach monitoring a temperature in a first core of the processor. Thus, Shakkarwar in view of

Rogenmoser does not teach or suggest all limitations of claim 22. Accordingly, Appellant respectfully asserts that the rejection is improper and requests that it be reversed.

C. Claims 5, 15, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shakkarwar in view Korean Patent Publication 9405466 B1 to Kim (hereinafter "Kim).

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. Without conceding that the second criteria is satisfied, the Appellant respectfully asserts that the Examiner's rejection fails to satisfy the first or third criteria.

Claim 5 depends from claim 1, claims 15 depends from claim 8, and claim 23 depends from claim 16. Each of claims 5, 15, and 23 inherit every limitation of the claims from which they depend. As shown above, Shakkarwar fails to teach or suggest "said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit." Moreover, Kim is not relied upon to teach or suggest this missing limitation. As such, claims 5, 15, and 23 set forth limitations not taught or suggested by the Examiner's proposed combination, and are allowable at least for the reasons set forth above with respect to claims 1, 8, and 16. Therefore, Appellant respectfully requests reversal of the rejection of record.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto in the Claims Appendix. As indicated above, the claims in Claims Appendix include the amendments filed by Appellant on June 21, 2006.

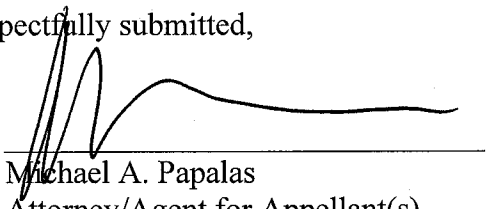
IX. EVIDENCE

No evidence pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the Examiner is being submitted. As such, no such evidence is included.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, and copies of decisions in related proceedings are not provided. No such related proceedings are included.

Respectfully submitted,

By: 

Michael A. Papalas
Attorney/Agent for Appellant(s)
Reg. No. 40,381
Date: February 14, 2007
Telephone No. (214) 855-8186

CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/644,625

1. A system comprising:

an integrated circuit on a VLSI die; and

an embedded micro-controller constructed on the VLSI die, the micro-controller adapted to monitor and control the VLSI environment to optimize the integrated circuit operation;

wherein said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit.

2. The system of claim 1 wherein the embedded micro-controller also monitors one or more of the parameters selected from the group consisting of:

the power supplied to the integrated circuit;

the operating clock frequency of the integrated circuit;

the power supply voltage; and

the power supply current supplied to the integrated circuit.

3. The system of claim 1 wherein the embedded micro-controller controls at least one of the following parameters:

temperatures at one or more locations on the integrated circuit;

the integrated circuit power supply;

the operating clock frequency of the integrated circuit;

the power supply voltage; and

the power supply current supplied to the integrated circuit.

4. The system of claim 1 wherein the integrated circuit comprises two or more processor cores, each core having a integer unit and a floating point unit, the micro-controller further comprising:

temperature sensors at each of the integer units and floating point units on each of the cores.

5. The system of claim 1 further comprising:

embedded ammeters constructed on the VLSI integrated circuit die, the ammeters comprising voltage controlled oscillators.

6. The system of claim 1 further comprising:

fuses that provide hardware selection of VLSI integrated circuit environment parameters that are monitored by the embedded micro-controller.

7. The system of claim 1 further comprising:

updateable or replaceable firmware for controlling operations of the embedded micro-controller; said firmware comprising:

algorithms for determining how to respond to temperature, power, voltage, or clock parameters.

8. A method for monitoring and controlling an integrated circuit comprising:

providing an embedded micro-controller on a same VLSI die as the integrated circuit; and

monitoring and controlling a VLSI environment of the integrated circuit with the embedded micro-controller; wherein

said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit.

9. The method of claim 8 further comprising:

also monitoring, by the embedded micro-controller, one or more integrated circuit parameters selected from the group consisting of:

the power supplied to the integrated circuit;

the operating clock frequency of the integrated circuit;

the power supply voltage; and

the power supply current supplied to the integrated circuit.

10. The method of claim 8 further comprising:

controlling, by the embedded micro-controller, one or more processor parameters selected from the group consisting of:

temperatures at one or more locations on the integrated circuit;

the integrated circuit power supply;

the operating clock frequency of the integrated circuit;

the power supply voltage; and

the power supply current supplied to the integrated circuit.

11. The method of claim 8 further comprising:

controlling, using the embedded micro-controller, the VLSI environment to optimize an integrated circuit operating power level to approach a design limit.

12. The method of claim 8 further comprising:

monitoring, using the embedded micro-controller, a temperature in a location of the integrated circuit; and

reducing, using the embedded micro-controller, a power supply voltage in response to an over-temperature condition in the location.

13. The method of claim 8 further comprising:

monitoring, using the embedded micro-controller, a temperature in a location of the integrated circuit; and

reducing, using the embedded micro-controller, a processor operating clock frequency in response to an over-temperature condition in the integrated circuit.

14. The method of claim 8 wherein the integrated circuit is a processor, the method further comprising:

monitoring, using the embedded micro-controller, a temperature in a first core of the processor; and

transferring, using the embedded micro-controller, a processing workload from the first core to a second core of the processor in response to the temperature of said first core.

15. The method of claim 8 further comprising:

monitoring, using the embedded micro-controller, current levels in the integrated circuit using ammeters comprising one or more voltage controlled oscillators.

16. A computer program product comprising a computer usable medium having computer readable program code embedded therein, the computer readable program code comprising:

code for controlling an embedded micro-controller constructed on a VLSI integrated circuit die with a processor, wherein the micro-controller monitors and controls a VLSI environment of the processor; where

said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit.

17. The computer program product of claim 16 further comprising:

code for also monitoring, by the embedded micro-controller, one or more integrated circuit parameters selected from the group consisting of:

the power supplied to the integrated circuit;

the operating clock frequency of the integrated circuit;

the power supply voltage; and

the power supply current supplied to the integrated circuit.

18. The computer program product of claim 16 further comprising:

code for controlling, by the embedded micro-controller, one or more integrated circuit parameters selected from the group consisting of:

temperatures at one or more locations on the integrated circuit;

the integrated circuit power supply;

the operating clock frequency of the integrated circuit;

the power supply voltage; and

the power supply current supplied to the integrated circuit.

19. The computer program product of claim 16 further comprising:

code for controlling the VLSI environment to optimize an integrated circuit operating power level to approach a design limit.

20. The computer program product of claim 16 further comprising:

code for monitoring a temperature in a core of the processor; and

code for reducing a power supply voltage in response to an over-temperature condition in the core.

21. The computer program product of claim 16 further comprising:

code for monitoring a temperature in a core of the processor; and

code for reducing a processor operating frequency in response to an over-temperature condition in the core.

22. The computer program product of claim 16 further comprising:

code for monitoring a temperature in a first core of the processor; and

code for transferring a processing workload from the first core to a second core of the processor in response to the temperature of said first core.

23. The computer program product of claim 16 further comprising:

code for monitoring current levels in the integrated circuits using ammeters comprising one or more voltage controlled oscillators.

24. A system for monitoring and controlling an integrated circuit comprising:

means for providing an embedded micro-controller on a same VLSI die as the integrated circuit; and

means for monitoring and controlling a VLSI environment of the integrated circuit with the embedded micro-controller;

wherein said embedded micro-controller monitors temperatures at a plurality of locations on the integrated circuit.

25. The system of claim 24 further comprising:

means for controlling, using the embedded micro-controller, the VLSI environment to optimize an integrated circuit operating power level to approach a design limit.

26. The system of claim 24 further comprising:

means for reducing, using the embedded micro-controller, a power supply voltage in response to an over-temperature condition at one of said plurality of locations.

27. The system of claim 24 further comprising:

means for reducing, using the embedded micro-controller, a processor operating clock frequency in response to an over-temperature condition in the integrated circuit.

28. The system of claim 24 wherein the integrated circuit is a processor, the method further comprising:

means for monitoring, using the embedded micro-controller, a temperature in a first core of the processor; and

means for transferring, using the embedded micro-controller, a processing workload from the first core to a second core of the processor in response to the temperature of said first core.

29. The system of claim 1 wherein

said embedded micro-controller is further adapted to detect a difference in temperatures between said plurality of locations on the integrated circuit and redistribute workload in response to said temperature difference.

30. The method of claim 8 wherein

said embedded micro–controller detects a difference in temperatures between said plurality of locations on the integrated circuit and redistributes workload in response to said temperature difference.

31. The computer program product of claim 16 where

said embedded micro–controller detects a difference in temperatures between said plurality of locations on the integrated circuit and redistributes workload in response to said temperature difference.

32. The system of claim 24 where

said embedded micro–controller detects a difference in temperatures between said plurality of locations on the integrated circuit and redistributes workload in response to said temperature difference.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None